CMOS 4-BIT MICROCONTROLLER

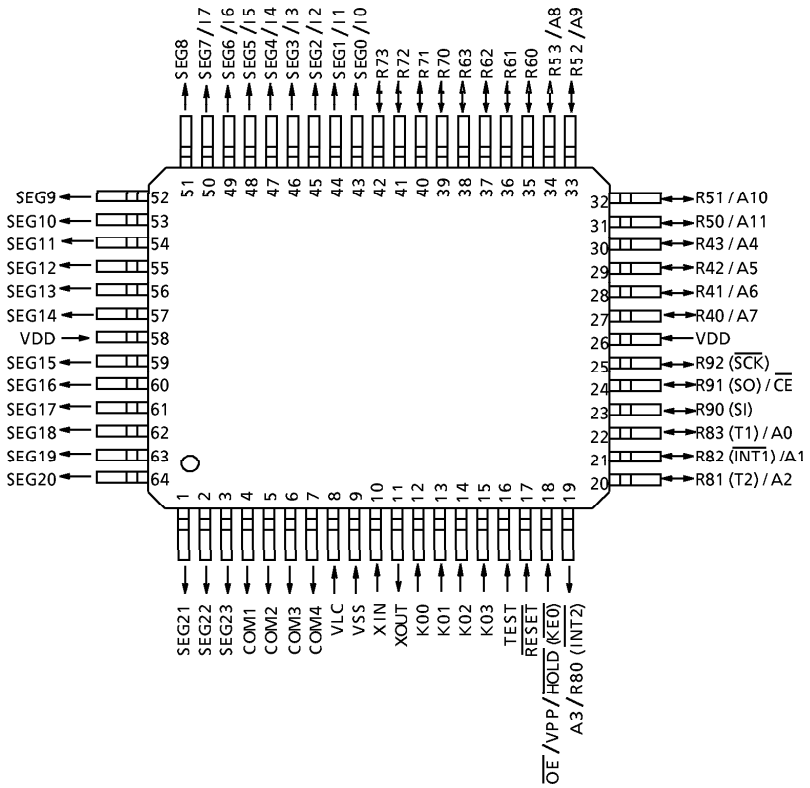
TMP47P421ADF

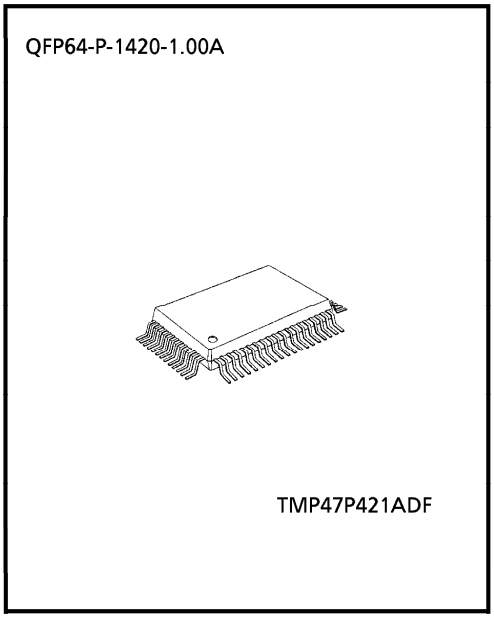
The 47P421A is the system evaluation LSI of 47C221A/421A with 32K bits one-time PROM. The 47P421A programs / verifies using an adapter socket to connect with PROM programmer, as it is in 2732AD.
In addition, the 47P421A and the 47C221A/421A are pin compatible. The 47P421A operates as the same as the 47C221A/421A by programming to the internal PROM.

PART No.	ROM	RAM	PACKAGE	ADAPTER SOCKET
TMP47P421ADF	OTP 4096 × 8-bit	256 × 4-bit	QFP64-1420-1.00A	BM1114A

PIN ASSIGNMENT (TOPVIEW)

QFP64-P-1420-1.00A





PIN FUNCTION

The 47P421A has MCU mode and PROM mode.

(1) MCU mode
The 47C221A/421A and the 47P421A are pin-compatible (TEST pin for out-going test. Be fixed to low level).

(2) PROM mode

PIN NAME	INPUT / OUTPUT	FUNCTIONS		PIN NAME (MCU MODE)
A11 to A8	INPUT	Address inputs		R50 to R53
A7 to A4				R40 to R43
A3 to A0				R80 to R83
I7 to I4	I/O	Data Outputs (Inputs)		SEG7 to SEG4
I3 to I0				SEG3 to SEG0
$\overline{CE}$	INPUT	Chip Enable input		R91
$\overline{OE}$ / VPP	Power Supply	Output Enable input	+ 21 V / 5 V / 0 V	$\overline{HOLD}$
VCC		+ 5 V		VDD
GND		0 V		VSS
VLC	Power Supply	Be fixed to low level.		
R63 to R60	I/O	Be fixed to low level.		
R73 to R70				
R92				
K03, K02	INPUT			
K01, K00				
R90	I/O	PROM mode setting pin. Be fixed to low level.		
$\overline{RESET}$	INPUT			
TEST		PROM mode setting pin. Be fixed to high level.		
SEG23 to SEG8	OUTPUT	Open		
COM4 to COM1				
XIN	INPUT	Resonator connecting pin.		
XOUT	OUTPUT			

OPERATIONAL DESCRIPTION

The following is an explanation of hardware configuration and operation in relation to the 47P421A. The 47P421A is the same as the 47C221A/421A except that an OTP is used instead of a built-in mask ROM.

1. OPERATION mode

The 47P421A has an MCU mode and a PROM mode.

1.1 MCU mode

The MCU mode is set by fixing the TEST / VPP pin at the "L" level. Operation in the MCU mode is the same as for the 47C221A/421A, except that the TEST/VPP pin does not have built in pull-down resistor and cannot be used open.

1.1.1 Program Memory

The program storage area are as shown in Figure1-1.

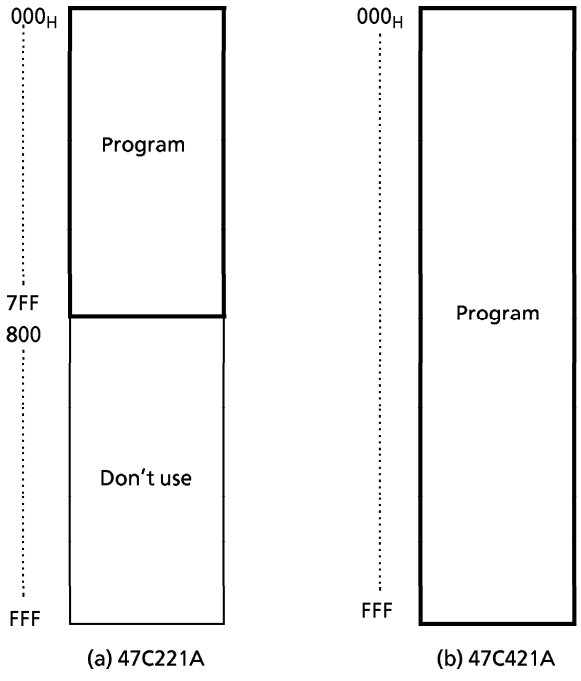


Figure 1-1. Program area (ROM)

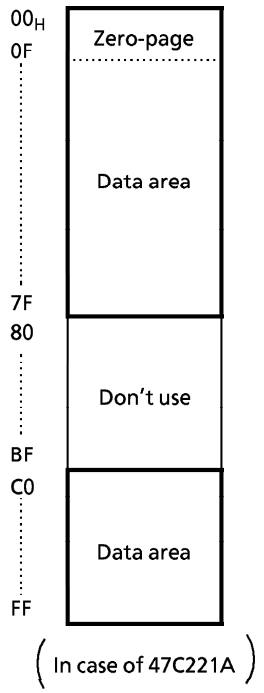


Figure 1-2. RAM addressing

1.1.2 Data Memory

The 47P421A contains 256 × 4-bit (equivalent to 47C421A) data memory. When the 47P421A is used as evaluator of the 47C221A, programming should be performed assuming that the RAM is assigned to addresses 00 to $7F_H$ and C0 to FF_H as show in Figure 1-2 by considering the application software evaluation.

1.1.3 Input / Output Circuitry

(1) Control pins
This is the same as for the 47C221A/421A except that there is no built-in pull-down resistance for the TEST pin.

(2) I/O Ports
The input/output circuit of the 47P421A is the same as I/O code GA of the 47C221A/421A.
External resistance, for example, is required when using as evaluator of other I/O codes (GB to GF), (Refer to Figure 1-3)

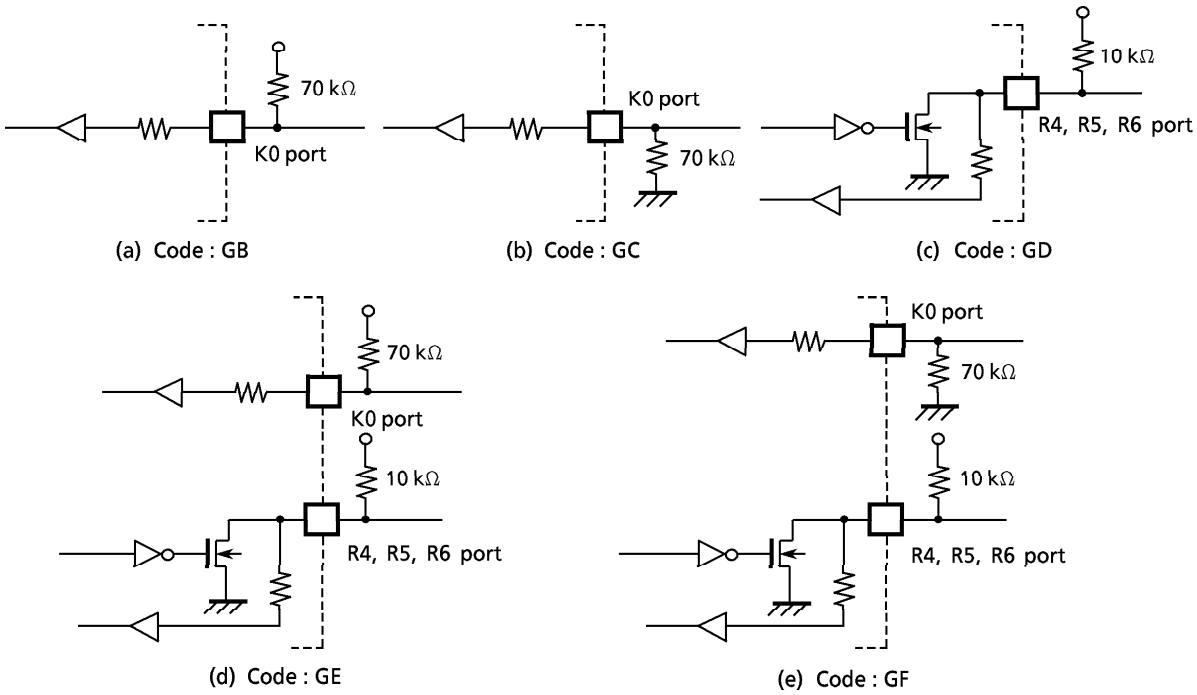
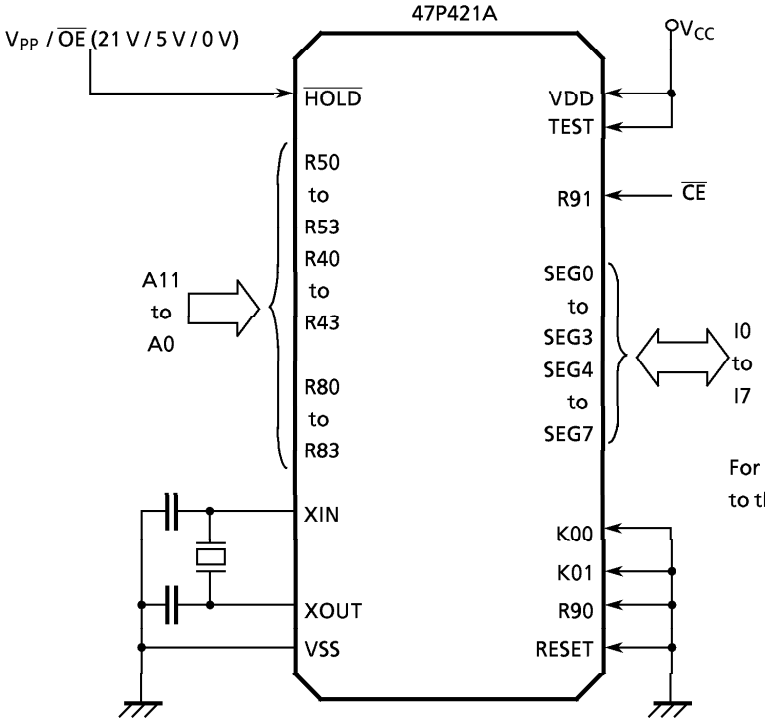


Figure 1-3. I/O code and external circuitry

1.2 PROM mode

The PROM mode is set by setting the $\overline{\text{RESET}}$, R90, K00 and K01 pins to the "L" level. The PROM mode can be used as a general-purpose PROM writer for program writing and verfication.

An adapter socket (part No. BM1114A) is available for connecting a PROM writer.



For more information on pins refer to the section on pin function.

Figure 1-4. Setting for PROM mode

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0 V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		– 0.5 to 7	V
Program Voltage	V_{PP}	Hold/V_{PP} pin	– 0.5 to 22.0	V
Supply Voltage (LCD drive)	V_{LC}		– 0.5 to V_{DD} + 0.5	V
Input Voltage	V_{IN}		– 0.5 to V_{DD} + 0.5	V
Output Voltage	V_{OUT1}	Except sink open drain pin	– 0.5 to V_{DD} + 0.5	V
	V_{OUT2}	Sink open drain pin	– 0.5 to 10	
Output Current (per 1 pin)	I_{OUT}		3.2	mA
Power Dissipation [T_{opr} = 70℃]	PD		400	mW
Soldering Temperature (time)	T_{sld}		260 (10 s)	°C
Storage Temperature	T_{stg}		– 55 to 125	°C
Operating Temperature	T_{opr}		– 30 to 70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0 V, T_{opr} = – 30 to 70 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		In the Normal operating mode	4.5	6.0	V
			In the Hold operating mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	VDD ≧ 4.5 V	VDD × 0.7	V_{DD}	V
	V_{IH2}	Hysteresis Input		VDD × 0.75		
	V_{IH3}		VDD < 4.5 V	VDD × 0.9		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	VDD ≧ 4.5 V	0	V_{DD} × 0.3	V
	V_{IL2}	Hysteresis Input			V_{DD} × 0.25	
	V_{IL3}		VDD < 4.5 V		V_{DD} × 0.1	
Clock Frequency	fc			0.4	4.2	MHz

Note 1. Input Voltage V_{IH3}, V_{IL3} : in the HOLD operating mode.
Note 2. 1MHz is recommended as minimum freqency when SLF = 1. And 2MHz is when SLF = 0.

D.C. CHARACTERISTICS (V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = – 30 to 70 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		—	0.7	—	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5 V, V_{IN} = 5.5 V / 0 V	—	—	± 2	μA
	I_{IN2}	Open drain R port					
Input Low Current	I_{IL}	Push-pull R port	V_{DD} = 5.5 V, V_{IN} = 0.4 V	—	—	– 2	mA
Input Registance	R_{IN2}	$\overline{RESET}$		100	220	450	kΩ
Output Leakage Current	I_{LO}	Open drain port R	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	—	—	2	μA
Output High Voltage	V_{OH}	Push-pull R port	V_{DD} = 4.5 V, I_{OH} = – 200 μA	2.4	—	—	V
Output Low Voltage	V_{OL}	Except XOUT	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	—	—	0.4	V
Segment Output Low Registance	R_{OS1}	SEG pin	V_{DD} = 5 V, V_{DD} – V_{LC} = 3 V	—	10	—	kΩ
Common Output Low Registance	R_{OC1}	COM pin					
Segment Output High Resistance	R_{OS2}	SEG pin		—	70	—	kΩ
Common Output High Resistance	R_{OC2}	COM pin					
Segment/Common Output Registance	$V_{O2/3}$	SEG / COM pin		3.8	4.0	4.2	V
	$V_{O1/2}$			3.3	3.5	3.7	
	$V_{O1/3}$			2.8	3.0	3.2	
Supply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5 V, V_{LC} = V_{SS} fc = 4 MHz	—	5	10	mA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5 V	—	0.5	10	μA

Note 1. Typ. values show those at T_{opr} = 25 °C, V_{DD} = 5 V.
Note 2. Input Current I_{IN1} ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.
Note 3. Output Resistance R_{OS}, R_{OC} ; Shows on-resistance at the level switching.
Note 4. $V_{O2/3}$; Shows 2/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.
Note 5. $V_{O1/2}$; Shows 1/2 level output voltage, when the 1/2 duty or static LCD is used.
Note 6. $V_{O1/3}$; Shows 1/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.
Note 7. Supply Current I_{DD}, I_{DDH} ; V_{IN} = 5.3 V /0.2 V
The K0 port is open when the input resistor is contained.
The voltage applied to the R port is within the valid range.
Note 8. When using LCD, it is necessary to consider values of $R_{OS1/2}$ and $R_{OC1/2}$.
Note 9. Times for SEG / COM output resistance switching on :
R_{OS1}, R_{OC1} : 2/fs (s)
R_{OS2}, R_{OC2} : 1/(n·f_F) (1/n : duty, f_F : frame frequency)

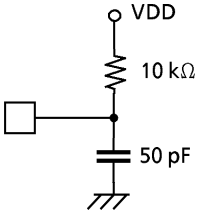
A.C. CHARACTERISTICS

(V_{SS} = 0 V, V_{DD} = 4.5 to 6.0 V, T_{opr} = – 30 to 70 °C)

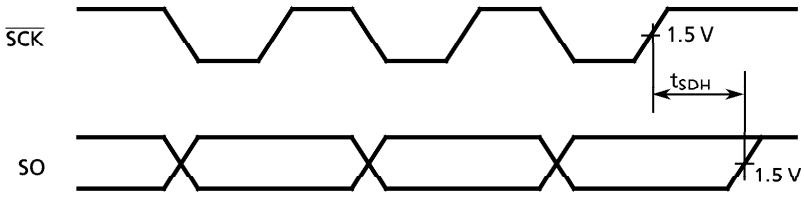
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}		1.9	—	20	μs
High level Clock pulse Width	t_{WCH}	External clock mode	80	—	—	ns
Low level Clock pulse Width	t_{WCL}					
Shift data Hold Time	t_{SDH}		0.5 t_{cy} – 300	—	—	ns

Note. Shift data Hold Time:

External circuit for $\overline{SCK}$ pin and SO pin



Serial port (completion of transmission)

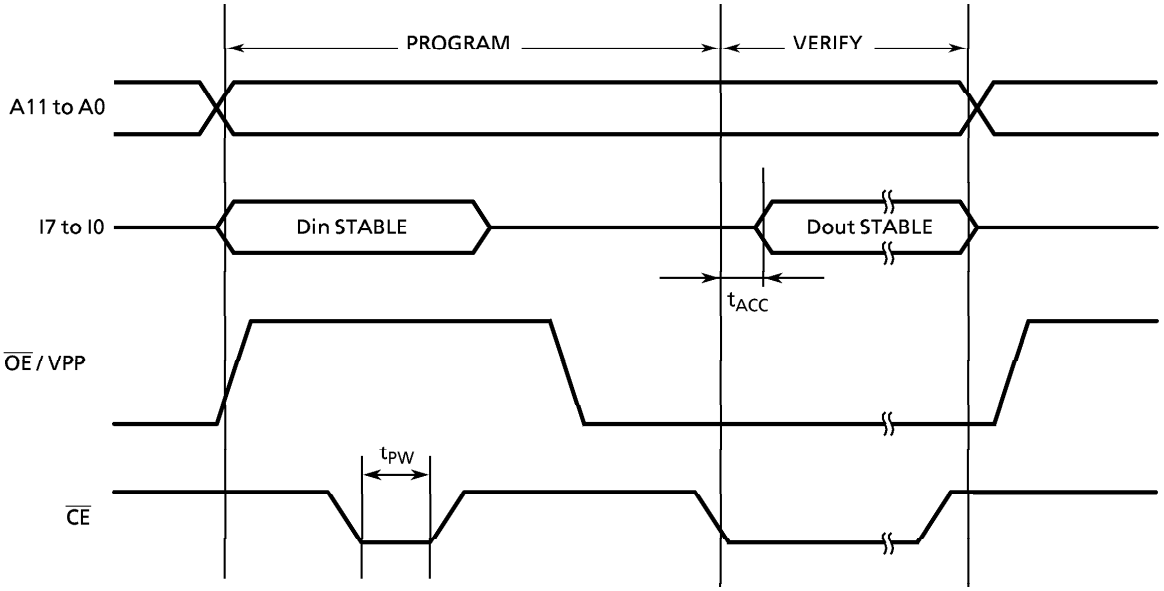


RECOMMENDED OSCILLATING CONDITIONS

Recommended oscillating conditions of the 47P421A are equal to the 47C221A/421A's.

D.C./A.C. CHARACTERISTICS (PROM mode) (V_{SS} = 0 V)

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Output Level High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Output Level Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.12$	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
Programming Voltage	V_{PP}	Verify				
		Program	20.5	21.0	21.5	
Address Access Time	t_{ACC}	V_{CC} = 5.0 ± 0.25 V	0	–	350	ns
Programming Pulse Width	t_{PW}		0.95	1.0	1.05	ms



※ Difference compared with the 47C221A/421A.
The 47P421A is different from the 47C221A/421A with respect to the following spec points.

PARAMETER	SYMBOL	CONDITION	TMP47C221A / 421A			TMP47P421AD			UNIT
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Voltage	V_{DD}	In the NORMAL operation	4.5	–	6.0	4.5	–	6.0	V
Supply Current	I_{DD}		–	3	6	–	5	10	mA

Note. Be fixed low level at MCU mode because of TEST pin does not have pull-down resistor.

TYPICAL CHARACTERISTICS